The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LEONARD FORBES,
JOSEPH E. GEUSIC and KIE Y. AHN

Appeal No. 2005-1281
Application 09/134,713

ON BRIEF

Before WARREN, OWENS and WALTZ, *Administrative Patent Judges*.

WARREN, *Administrative Patent Judge*.

Decision on Appeal

This is an appeal under 35 U.S.C. § 134 from the decision of the examiner finally rejecting claims 22, 25 through 42 and 51 through 56. Claims 43 through 50 are also of record and have been withdrawn from consideration by the examiner under 37 CFR § 1.142(b).

Claims 26, 36, 38, 39, 41, 42, 55 and 56 illustrate appellants' invention of a method of forming a floating gate transistor having an amorphous carburized silicon insulative layer between the channel region of the substrate and the floating gate, and a method of forming a memory cell comprising forming the floating gate transistor, and are representative of the claims on appeal:

26. A method of forming a memory cell comprising:

forming a source region in a substrate;

forming a drain region in the substrate, a channel region being between the source region and the drain region in the substrate;

forming a floating gate; and

forming an amorphous silicon carbide (a-SiC) insulator between the floating gate and the channel region in the substrate.

36. A method for forming a transistor comprising:

forming a source region in a silicon substrate;

forming a drain region in the substrate;

forming a channel region in the substrate between the source region and the drain region; and

forming a floating gate separated from the channel region by an amorphous silicon carbide (a-SiC) insulator, wherein forming a floating gate further comprises forming at least one of the floating gate and the a-SiC insulator to have an electron affinity such that a barrier energy, defined as a difference between an electron affinity of the floating gate and an electron affinity of the a-SiC insulator, is less than approximately 3.3 eV.

38. The method of claim 36, further comprising forming a control electrode opposite from the floating gate and separated from the floating gate by an intergate insulator.

39. The method of claim 38 wherein forming a control electrode further comprises forming the control electrode with a shape such that an area of a capacitor formed by the control electrode, the floating gate, and the intergate insulator is larger than an area of a capacitor formed by the floating gate, the a-SiC insulator, and the channel region.

41. A method for forming a floating gate transistor, comprising:

forming a source and drain regions in a silicon substrate;

forming an amorphous silicon carbide (a-SiC) insulator over a channel region located between the source and drain regions in the substrate; and

forming a floating gate on the a-SiC insulator, wherein forming an amorphous silicon carbide (a-SiC) gate insulator and forming a floating gate further comprises forming the a-SiC insulator and forming the floating gate such that a barrier energy, defined as a difference between an electron affinity of the floating gate and an electron affinity of the a-SiC insulator, is less than approximately 3.3 eV.

42. The method of claim 41 wherein forming an amorphous silicon carbide (a-SiC) gate insulator further comprises forming an amorphous silicon carbide (a-SiC) gate insulator by ion-implantation of C_2H_2 into a silicon substrate.

55. A method for forming a floating gate transistor comprising:

forming a p-type source region and a p-type drain regions in a silicon substrate;

forming an amorphous silicon carbide (a-SiC) gate insulator over a channel region in the substrate, the channel region being located between the source and drain regions; and

forming a polysilicon floating gate on the a-SiC gate insulator.

56. The method of claim 55 wherein:

forming an amorphous silicon carbide (a-SiC) gate insulator further comprises forming the a-SiC gate insulator by ion-implantation of C_2-H_2 into the substrate to have an electron affinity that is less than an electron affinity of silicon dioxide (SiO_2);

forming a polysilicon floating gate further comprises forming the a-SiC gate insulator and forming the polysilicon floating gate such that a barrier energy, defined as a difference between an electron affinity of the polysilicon floating gate and an electron affinity of the a-SiC gate insulator, is less than approximately 3.3 eV; and

further comprising:

forming an intergate insulator on the polysilicon floating gate; and

forming a control electrode on the intergate insulator.

The references relied on by the examiner are:

Baldi	4,816,883	Mar. 28,1989
Jeong	5,886,379	Mar. 23, 1999
Sugita et al. (Sugita)[1] (Japanese Kokai Patent Publication)	08-255878	Oct. 1, 1996

I. Sakata et al. (Sakata), "Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures," 30 *Electronic Letters* no. 9, 688-89 (April 1994).

Compagnini et al. (Compagnini), "Spectroscopic Characterization of Annealed $Si_{1-x}C_x$ Films," 11 *Journal of Materials Research*, no. 9, 2269-73 (September 1996).

Appellants have relied on the following references:

Q.-D. Qian et al. (Qian), "Multi-day Dynamic Storage of Holes at the AlAs/GaAs Interface," EDL-7 *IEEE Electron Device Letters* no. 11, 607-09 (November 1986).

Stanley G. Burns et al. (Burns), "Semiconductor Memories," *Principles of Electronic Circuits* 382-83 (St. Paul, West Publishing Company. 1987).

Federico Capasso et al. (Capasso), "New Floating-Gate AlGaAs/GaAs Memory Devices with Graded-Gap Electron Injector and Long Retention Times," 9 *IEEE Electron Device Letters* no. 8, 607-09 (August 1988).

[1] We refer in our decision to the translation of Sugita submitted by appellants with the IDS filed July 2, 1999.

J.A. Lott et al. (Lott), "Anisotropic thermionic emission of electrons contained in GaAs/AlAs floating gate device structures," 55 *Appl. Phys. Lett.*, no. 12, 1226-28 (September 1989).

The examiner has advanced the following grounds of rejection on appeal:

claims 22, 25 through 38, 40, 41, 51 and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakata in view of Sugita (answer, pages 3-4);

claim 39 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakata in view of Sugita as applied to claims 22, 25 through 38, 40, 41, 51 and 53, and further in view of Jeong (answer, pages 4-5);

claims 42, 52 and 54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakata in view of Sugita as applied to claims 22, 25 through 38, 40, 41, 51 and 53, and further in view of Compagnini (answer, pages 5-6);

claim 55 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakata in view of Sugita as applied to claims 22, 25 through 38, 40, 41, 51 and 53, and further in view of Baldi (answer, page 6); and

claim 56 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakata in view of Sugita and further in view of Baldi as applied to claim 55, and further in view of Compagnini (answer, page 7).

Appellants group the appealed claims based on the grounds of rejection and separately argue claims 26, 39, 42, 55 and 56 (brief, pages 3, 5 and 14). Thus, we decide this appeal based on these appealed claims. 37 CFR § 1.192(c)(7) (2003); *see also* 37 CFR § 41.37(c)(1)(vii) (September 2004).

We affirm.

Rather than reiterate the respective positions advanced by the examiner and appellants, we refer to the answer and to the brief and reply brief for a complete exposition thereof.

Opinion

We have carefully reviewed the record on this appeal and based thereon find ourselves in agreement with the supported position advanced by the examiner that, *prima facie*, the claimed method of forming a memory cell encompassed by appealed claim 26 would have been obvious over the combined teachings of Sakata and Sugita to one of ordinary skill in this art at the time the claimed invention was made. In view of the established *prima facie* case of obviousness, we again consider the record as a whole with respect to this ground of rejection in light of appellants' rebuttal arguments in the brief and reply brief. *See generally, In re Oetiker*, 977 F.2d

1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984).

Our consideration of the application of the cited prior art to claim 26 requires that we first interpret the claim language thereof by giving the claim terms their broadest reasonable interpretation in light of the written description in the specification as interpreted by one of ordinary skill in the art, without reading into the claim any limitation or particular embodiment disclosed in the specification. *See, e.g., In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). The plain language of claim 26 encompasses a method of forming a memory cell comprising at least the steps of forming source and drain regions and thus, a channel region therebetween, in any substrate and forming a layer of amorphous carburized silicon, that is, amorphous silicon carbide (a-SiC), between the channel region and a floating gate which is also formed. The transitional term "comprising" opens claim 26 to include additional step or steps employing any manner of additional materials to form any manner of an additional elements or layer(s) including a control gate formed adjacent to and insulated from the floating gate, as well as electrodes on the source and drain regions and the control gate, and indeed, any other elements of any manner of memory cell, including the floating gate transistors formed by such methods as encompassed by appealed claim 42, for example. *See*, e.g., *Vehicular Technologies Corp. v. Titan Wheel Int'l Inc.*, 212 F.3d 1377, 1383, 54 USPQ2d 1841, 1845 (Fed. Cir. 2000); *Exxon Chem. Pats., Inc. v. Lubrizol Corp.*, 64 F.3d 1553, 1555, 35 USPQ2d 1801, 1802 (Fed. Cir. 1995) ("The claimed composition is defined as comprising - meaning containing at least - five specific ingredients."); *In re Baxter*, 656 F.2d 679, 686-87, 210 USPQ 795, 802-03 (CCPA 1981) ("As long as one of the monomers in the reaction is propylene, any other monomer may be present, because the term 'comprises' permits the *inclusion* of other steps, elements, or materials.").

We find that Sakata would have disclosed to one of ordinary skill in this art a method of forming an aluminum (Al) ohmic contact/n- or p-type crystalline Si (c-Si)/graded hydrogenated amorphous silicon carbide (a-SiC:H)/ hydrogenated amorphous silicon (a-Si:H)/a-SiC:H/Al metal gate diode, wherein a graded a-SiC:H film, an a-Si:H film and an a-SiC:H film are formed

on an n- or p- type c-Si substrate followed by the formation of the Al metal gate and the Al ohmic contacts (Sakata **Fig. 1** and "*Sample Preparation*," page 688). Sakata would have further disclosed that experiments with such devices resulting in the "*Capacitance-voltage characteristics*" of a sample diode having an n-type substrate shown in Sakata **Fig. 2**, "confirm that the [a-SiC:H/a-Si:H heterojunctions] structure shown in **Fig. 1** can be applied to floating-gate memory devices" which operate as follows:

> With the application of positive (negative) bias to the metal gate, electrons (holes) are efficiently injected from the crystalline Si (c-Si) substrate into the thin a-Si:H layer through the compositionally graded a-SiC:H layer. When the bias voltage is restored to zero, injected electrons(holes) can be stored in the a-Si:H layer because of the discontinuity of the conduction (valence) band edges at the a-SiC:H/a-Si:H interfaces. By applying a negative (positive) gate bias, holes (electrons) are injected from the substrate into the a-Si:H layer through the graded a-SiC:H layer and recombine with the stored electrons and thus the memory is erased. [Page 688, cols. 1-2.]

Sakata reports the basis for this in "*Results and discussion*," suggesting that the graded a-SiC:H/a-Si:H "structure can be used as a component of dynamic random access memories (DRAMs) at room temperature [footnote omitted.]" (pages 688-89). Sakata states in "*Conclusion*" that "band-engineered a-Si:H/a-SiC:H heterojunctions on c-Si can be applied to electrically programmable and erasable memory devices because both electrons and holes can be conducted through undoped a-SiC:H and can be stored in a-Si:H" as "[i]t has been confirmed that the graded a-SiC:H and the a-Si:H act as the carrier injection layer and the memory trap site, respectively" (page 689).

We find that Sugita would have disclosed to one of ordinary skill in this art floating gate transistors such as that illustrated in Sugita **Fig. 1** in which polycrystalline silicon carbide (β-SiC) insulating layer **5** can be grown on a p-type silicon substrate **1** over the channel region between source region **2** and drain region **3**, after which SiO_2 layer **4** is formed at the interface between silicon substrate **1** and β-SiC layer **5**, thus separating the channel region from polysilicon floating gate **6** which is isolated from control grate **8** by SiO_2 layer **7**, and with source electrode **9**, drain electrode **10** and an electrode on control gate **8** as shown; and would have acknowledged in **Fig. 3**, a "conventional floating gate transistor" which differs from that of Sugita **Fig. 1** in the absence of SiO_2 layer **4** (pages 2-3, 7-8, 10-11 and 16-19). Sugita would have further disclosed

particular steps of forming the n-type source and drain regions, the β-SiC layer on the substrate between the floating gate and the channel region, and the control gate (pages 10-11).

We find that the conventional floating gate transistor acknowledged by Sugita and floating gate transistors disclosed in this reference differ from the claimed memory cell prepared by the method of claim 26 in the presence of β-SiC rather than a-SiC. However, Sugita would have disclosed to this person that the silicon carbide (SiC) layer can be any form of SiC (e.g., page 7, [0017]), and particularly that "in the above–mentioned application example [at pages 10-11, referring to **Fig. 1**], polycrystalline β-SiC is used as the SiC component of the gate insulating film" but "a polycrystalline crystal need not be used: *amorphous* . . . may also be adopted" (page 13, [0041]; italics emphasis added).[2]

We find that the acknowledged conventional floating gate transistor and the disclosed floating gate transistors are taught by Sugita to operate as a component of a cell of a DRAM integrated circuit memory device, wherein the electron barrier between the silicon substrate and an SiC film grown on the substrate is adjusted with an SiO_2 layer to permit tunnel conduction and provide an appropriate refresh time (e.g., pages 4-6, 8-9 and 11-12). In this respect, the SiO_2 layer of the disclosed floating gate transistor which can be formed in the silicon substrate after the SiC film is formed on that substrate, is no more than 3 nm thick and has no insulative properties (e.g., page 8, [0019] and [0020], page 9, [0025], and page 11, [0033]).

The examiner finds that the a-SiC:H layer containing device having an Al contact on each end disclosed by Sakata for application to floating gate memory devices, differs from the claimed method encompassed by claim 26 in the absence of the formation of source, drain and channel regions in the n- or p- type c-Si substrate of that device (answer, page 4). The examiner determines that one of ordinary skill in the art would have formed such regions in the c-Si substrate of Sakata as suggested by the formation of the same regions in the p-type silicon substrates of the floating gate transistors taught by Sugita in the expectation of successfully

[2] It is well settled that a reference stands for all of the specific teachings thereof as well as the inferences one of ordinary skill in this art would have reasonably been expected to draw therefrom, *see In re Fritch*, 972 F.2d 1260, 1264-65, 23 USPQ2d 1780, 1782-83 (Fed. Cir. 1992); *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968), presuming skill on the part of this person. *In re Sovish*, 769 F.2d 738, 743, 226 USPQ 771, 774 (Fed. Cir. 1985).

modifying the method and thus the device of Sakata to form a floating gate transistor useful as a component in a floating gate memory cell in the same or similar manner as the floating gate transistors of Sugita (*id.*).

Appellants submit that "[t]here is no suggestion or motivation to form a device by combining elements from" Sakata and Sugita. In this respect, appellants first contend that "there are substantial difference between the principles of operation of the floating gate transistor of Sakata" which conducts "both electrons and holes" and "the principles of operation of the floating gate transistor of Sugita" (brief, pages 7-8). While appellants contend that "[t]he known principles of operation of a floating gate transistor such as Sugita are substantially different," they then discuss the teachings of Burns, arguing that "[u]nlike the operation of the HJ diode structure of Sakata, only electrons are involved in programming and erasing a floating gate transistor according to Burns" (brief, page 8).

We find here that while Burns would not have disclosed to one of ordinary skill in this art a method of forming a memory cell, the reference would have disclosed to this person that erasable programmable read-only memories (EPROMs) comprising an n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) having a source region and a drain region in a p-type substrate, an insulative gate oxide layer, a floating gate, an insulating layer and a select gate as shown in Burns **Fig. 9.10(b)** (page 382). We find that the "select gate" of Burns is functionally equivalent to the "control gate" of Sugita. Burns would have taught that when "a high voltage . . . is applied to the drain and to the select gate . . . [a] channel is established" such that "[e]lectrons are accelerated in the high field between source and drain, and acquire enough energy to enter the conduction band of the gate oxide layer" where "they are attracted by the positive potential on the select gate, and many of them lodge on the floating gate," thus trapping electrons on the floating gate when the voltage is removed (pages 382-83). Burns further teaches that illuminating the device with ultraviolet light, the trapped electrons obtain sufficient photon energy to escape the floating gate through the oxide layer (page 383).

Appellants further argue that adding the regions proposed by the examiner to the device of Sakata would change "the basic principles under which the Sakata construction was designed to operate," and that there is no evidence that such principles would not be changed (*id.*).

Appellants then contend that Sakata suggests that the structure shown therein can be used in a DRAM device, relying on Qian (brief, pages 8-9). In view of the clear suggestion that we find in Sakata in this respect (*see above* p. 6), it is not necessary that we discuss Qian.

Appellants next submit in this respect that Sakata's statement suggesting that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices" is not a clear teaching that would have motivated one of ordinary skill in the art to modify Sakata's device as proposed by the examiner, and contends that Sakata "teaches away from" the combination of Sakata, Sugita and Burns (brief, page 9). Appellants point to Sakata's reference to Capasso as reporting "similar memory devices based on AlGaAs/GaAs HJ," and allege that thus "Sakata is referring to the earlier statement in the same paragraph . . . that 'the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices'" (brief, pages 9-10). Appellants state that "Capasso reports AlGaAs/GaAs floating-gate memory devices" but "does not show a picture of the device," quoting the following part of Capasso's abstract with respect to the operation of such devices:

> Compared with conventional Si-based floating-gate devices this structure operates on a different injection method. Electrons are injected from the control gate into the floating gate using an AlGaAs graded-gap barrier. [Capasso, page 377, col. 1; brief, page 10.]

Appellants contend that Sakata thus would have indicated to one of ordinary skill in the art "that a floating gate device with its heterojunction operates like Capasso's memory device that injects electrons from the control gate into the floating gate" (brief, page 10). Appellants argue that this is a different principle of operation than taught by Burns as well as by Sugita who "describes tunnel conduction at the interface between the silicon substrate 1 and the SiC film 5 in paragraphs [0019] and [0020]" and "electrons stored in the cell 22 escape to the source and drain side by Fowler-Nordheim type tunnel injection in paragraph [0040]," wherein "source 2 and drain 3 are shown in the silicon substrate 1 of Sugita" (brief, page 10).

Appellants further rely on Lott in this respect, stating that "Lott refers to the [GaAs/AlAs floating gate device therein] as '[o]ur vehicle (Fig. 1) has a vertical structural similar to that of [Capasso]'" (brief, pages 10-11). Appellants describe the GaAs/AlAs floating gate device of Lott as "[t]he floating . . . is between the source and drain on one side and the channel on the

other side [of a superlattice], and separates the source and the drain from the channel" (brief, pages 11-12). Appellants allege that "[t]he transistor structure shown in Figure 1 of Lott is linked by Sakata and Lott through Capasso to Sakata's earlier statement that 'the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices" (brief, pages 11-12). On this basis, appellants advance the position that the alleged connection between the floating gate devices of the references is evidence to one of ordinary skill in the art "to use the heterojunction of Sakata in a transistor such as Lott's," and thus that "[t]he structures of Lott and Sugita are substantially different, and there is no comparable suggestion in the prior art to form a device combining elements from Sakata, Sugita and Burns" (brief, page 12).

The examiner responds that the combined teachings of Sakata and Sugita provide a sufficiently reasonable expectation of success, as absolute predictability is not required (answer, page 8). In this respect, the examiner points out that the c-Si, a-SiC:H and a-Si:H layers of the device of Sakata corresponds to substrate **1**, insulating layer **5** and floating gate **6**, respectively, of the floating gate transistor memory devices of Sugita; that Sakata suggests the use of the device in floating gate memory devices; and that Sugita shows source, drain and channel regions in floating gate memory devices (answer, pages 8-9). The examiner further argues that the principle of operation of the devices of Sakata and Sugita are not dissimilar, pointing out that the metal gate of Sakata is functionally similar to control gate **8** of Sugita; the a-SiC:H insulating layer of Sakata functions similar to insulating layer **5** of Sugita; and the a-Si:H layer of Sakata functions similar to floating gate **6** of Sugita.

Appellants reply that Sakata's statement that the HJ structure therein is applicable to floating gate memory devices is not established by the examiner's reliance on Sugita because Lott "is evidence that devices categorized as floating gate devices do not necessarily have the structure of Sugita" (reply brief, pages 1-2). Appellants further contend that there is no evidence that the device of Sakata having a source and drain of the device of Sugita "would be able to inject holes from the Si substrate into 'the thin a-Si:H layer through the compositionally graded a-SiC:H layer," and thus, "the addition of the source and drain would require a change in the basic principles under which the Sakata construction was designed to operate" (reply brief, pages 2-3).

Our consideration of the record as a whole in light of appellants' arguments leads us to agree with the examiner. Appellants disclose in the written description in their specification that the principal element of the memory cell formed by the method encompassed by claim 26 that is different from floating gate transistors of the prior art used in integrated circuit memory devices is the layer of a-SiC formed between the channel region of the substrate and the floating gate (e.g., pages 1-4, particularly, page 4, ll. 2-5). In this respect, we find that the closest applied prior art is Sugita which would have taught forming an a-SiC layer between the channel region of the substrate and the floating gate in preparing a floating gate transistor component for a DRAM integrated circuit memory device (*see above* pp. 6-7). Thus, the a-SiC layer containing floating gate transistors of Sugita satisfy all of the elements of claim 26.

In similar manner to the a-SiC layer containing floating gate transistor of Sugita, the device of Sakata **Fig. 1** has an a-SiC:H layer formed on a c-Si substrate that has an ohmic contact on its backside, and an electrode on the metal gate, which device is suggested by the reference to be used as a component in DRAM integrated circuit memory devices (*see above* pp. 5-6). Both references similarly describe the operation of the devices disclosed therein as the application of voltage to the substrate and the control or metal gate causes electrons in the substrate to enter the a-SiC or a-SiC:H insulative layer and lodge in the polysilicon or a-Si:H floating gate.

Thus, we are of the view that as the examiner contends, the combined teachings of Sakata and Sugita would have reasonably suggested to one of ordinary skill in this art that the substrate of the floating gate device of Sakata can be modified to have the electrode on the substrate in a source region which is paired with drain and channel regions formed therein by the method taught in Sugita to prepare a structurally related floating gate electrode, in the reasonable expectation of forming a floating gate transistor having an a-SiC:H layer formed between the substrate and the floating gate, which can be used as a memory cell component of a DRAM integrated circuit memory device. We are reinforced in our view by Burns, relied on by appellants,[3] which would have taught one of ordinary skill in the art that a floating gate transistor

[3] *See In re Hedges*, 783 F.2d 1038, 1039-40, 228 USPQ 685, 686 (Fed. Cir. 1986) ("In Hedges' case the Solicitor referred to new portions of the references cited by Hedges during examination for further support of the same rejection that had been upheld by the Board. Hedges had relied on these references before the Board, as he does before us, for his argument that viewed as a whole

with the same substrate having source, drain and channel regions operates in the same manner when a voltage is applied to the source region and the select, that is, control, gate, and can be used as a component of integrated circuit memory devices. *See In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981)("The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.").

We are not persuaded otherwise by appellants' arguments based on Capasso and Lott. We find no evidence in this record establishing that the device of Sakata "injects electrons from the control gate into the floating gate" as appellants contend based on a mere reference to Capasso by Sakata. We find that the statement of operation in the abstract of Capasso of a metal layer transistor structure, that appellants cannot otherwise identify except that it has control gate and floating gate functional structures, is directly contrary to the principle of operation stated by Sakata at page 688, col. 1, based on results discussed in Sakata for the disclosed silicon based floating gate structure. Indeed, the clear statement in Capasso's abstract that "[c]ompared with conventional Si-based floating-gate devices this structure operates on a different injection method" cannot be discounted in the absence in the record of a scientific explanation or additional evidence that address this point. We find no such explanation or evidence in Lott as relied on by appellants. Indeed, the metal layer floating gate structure of Lott appears to be similar to the metal layer floating gate structure of Capasso, and as appellants admit, the functional elements of the device of Lott are arranged differently than the functional elements of the silicon-based floating gate structure of Sakata. Thus, there is little, if any, evidence in the record supporting appellants allegation that the metal layer floating gate device disclosed in Lott is linked through the metal layer floating gate device of Capasso to the silicon based floating gate device of Sakata.

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the body of the prior art teaches away from conducting this reaction at high temperatures. The Solicitor should not be constrained from pointing to other portions of these same references in contravention of Hedges' position.").

We are also unpersuaded by appellants' arguments that the principle of operation of the silicon based floating gate device of Sakata described with respect to "electrons and holes" therein, differs from the principle of operation of the silicon based transistors of Sugita and indeed, of Burns which are described in each reference with respect to "electrons." We found above that the principles of operation is described in each of these references with respect to the application of voltage causing electrons in the substrate to enter the silicon based insulative layer and lodge in the silicon based floating gate. The fact that Sakata additionally describes the operation of the device therein in terms of electron holes while Sugita and Burns do not, does not alone establish a difference in the principles of operation of floating gate devices that are structurally related. Thus, the burden rests with appellants to submit scientific argument and/or objective evidence to establish their position. *See, e.g., In re Best*, 562 F.2d 1252, 1255-56, 195 USPQ 430, 433-34 (CCPA 1977)("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product. See *In re Ludtke*, [441 F.2d 660, 169 USPQ 563 (CCPA 1971)]. Whether the rejection is based on "inherency" under 35 USC § 102, on "prima facie obviousness" under 35 USC § 103, jointly or alternatively, the burden of proof is the same, and its fairness is evidenced by the PTO's inability to manufacture products or to obtain and compare prior art products. [Footnote and citation omitted.]"). In the absence of such scientific argument or evidence, appellants' mere arguments in this respect are entitled to little, if any, weight. *See In re De Blauwe*, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984); *In re Payne*, 606 F.2d 303, 315, 203 USPQ 245, 256 (CCPA 1979); *In re Lindner*, 457 F.2d 506, 508, 173 USPQ 356, 358 (CCPA 1972).

Thus, on this record, the combined teachings of Sakata and Sugita and indeed, Burns as relied on by appellants, provide substantial evidence in support of the examiner's position. Accordingly, we are of the opinion that one of ordinary skill in this art routinely following the combined teachings of Sakata and Sugita would have reasonably arrived at the claimed method of forming a memory cell encompassed by appealed claim 26, including each and every limitation thereof arranged as required therein, without resort to the written description in

appellants' specification. *See In re Dow Chem. Co.*, 837 F.2d 469, 473, 5 USPQ2d 1529, 1531 (Fed. Cir. 1988) ("The consistent criterion for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that [the claimed process] should be carried out and would have a reasonable likelihood of success viewed in light of the prior art. [Citations omitted] Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure.").

Furthermore, we found above that Sugita would have taught one of ordinary skill in this art that a-SiC can be used as an insulating layer in place of the β-SiC layer in the floating gate transistors of each of Sugita as illustrated **Fig. 1** and as acknowledged in **Fig. 3**, thus arriving at a-SiC containing floating gate transistors with a reasonable expectation of successfully using the same as a component of a memory cell in an integrated circuit memory devices. Therefore, one of ordinary skill in this art routinely following the teachings of Sugita alone would have reasonable arrived at the claimed method encompassed by claim 26, including each and every limitation arranged as required by the claim, without resort to the written description in appellants' specification and claims. *See B.F. Goodrich Co. v. Aircraft Braking Sys. Corp.*, 72 F.3d 1577, 1582, 37 USPQ2d 1314, 1318 (Fed. Cir. 1996) ("When obviousness is based on a particular prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference. [Citation omitted.] This suggestion or motivation need not be expressly stated. [Citation omitted.]"); *Merck & Co., Inc. v. Biocraft Labs., Inc.*, 874 F.2d 804, 807, 10 USPQ2d 1843, 1845-46 (Fed. Cir. 1989) ("That the '813 patent discloses a multitude of effective combinations does not render any particular formulation less obvious. This is especially true because the claimed composition is used for the identical purpose. [Citations omitted.]").

The ground of rejection of each of appealed claims 39, 42, 55 and 56 advanced by the examiner all rely on the combined teachings of Sakata and Sugita as further combined with Jeong, with Compagnini, with Baldi and with Baldi and Compagnini (answer, pages 4-7). While appellants point to the claim limitations in each of these claims which the examiner identifies in applying these combinations of reference(s), appellants only rely on the arguments we have considered above with respect to claim 55 or contend that there is no evidence for combining the

references with respect to claims 39, 42 and 56, in no case supporting their positions with evidence in the disclosures of the additional reference(s).

On this record, we have again considered the examiner's grounds of rejection involving claims 39, 42, 55 and 56 in light of appellants' contentions and based on the views that we have set forth above, agree with the examiner's positions.

Accordingly, based on our consideration of the totality of the record before us, we have weighed the evidence of obviousness found in the combined teachings of Sakata and Sugita, and as further combined with Jeong, with Compagnini, with Baldi, and with Baldi and Compagnini with appellants' countervailing evidence of and argument for nonobviousness and conclude that the claimed invention encompassed by appealed claims 22, 25 through 42 and 51 through 56 would have been obvious as a matter of law under 35 U.S.C. § 103(a).

The examiner's decision is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv) (September 2004).

AFFIRMED

CHARLES F. WARREN)
Administrative Patent Judge)
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)
TERRY J. OWENS) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
)
THOMAS A. WALTZ)
Administrative Patent Judge)

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